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Dixon/Usher  
Express Mail# ET 007354780  
8/14/2001

# ULIS Block Diagram

Paul K. Dixon 6/7/01

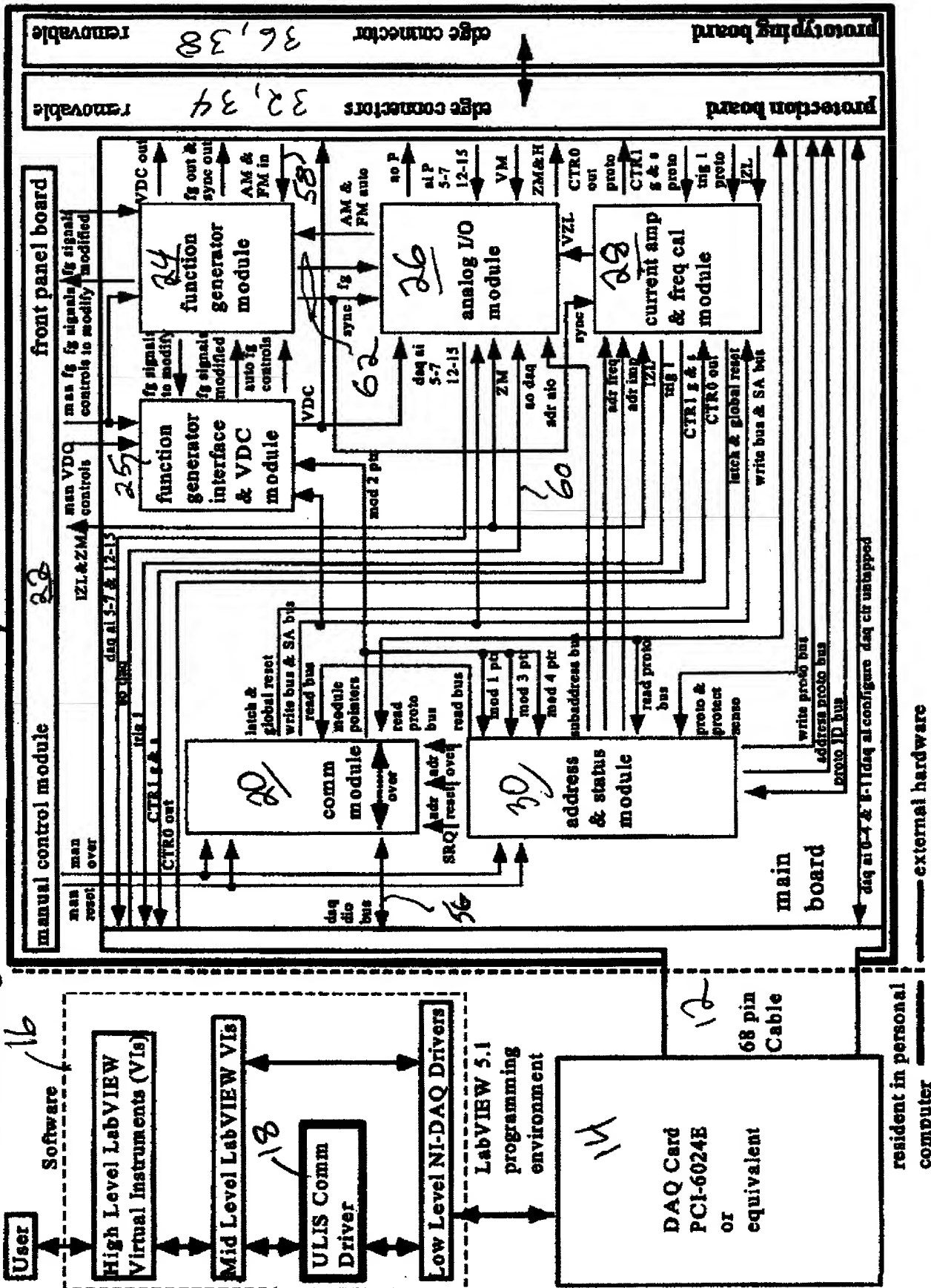


FIG. 1

T04T30" 0000E660

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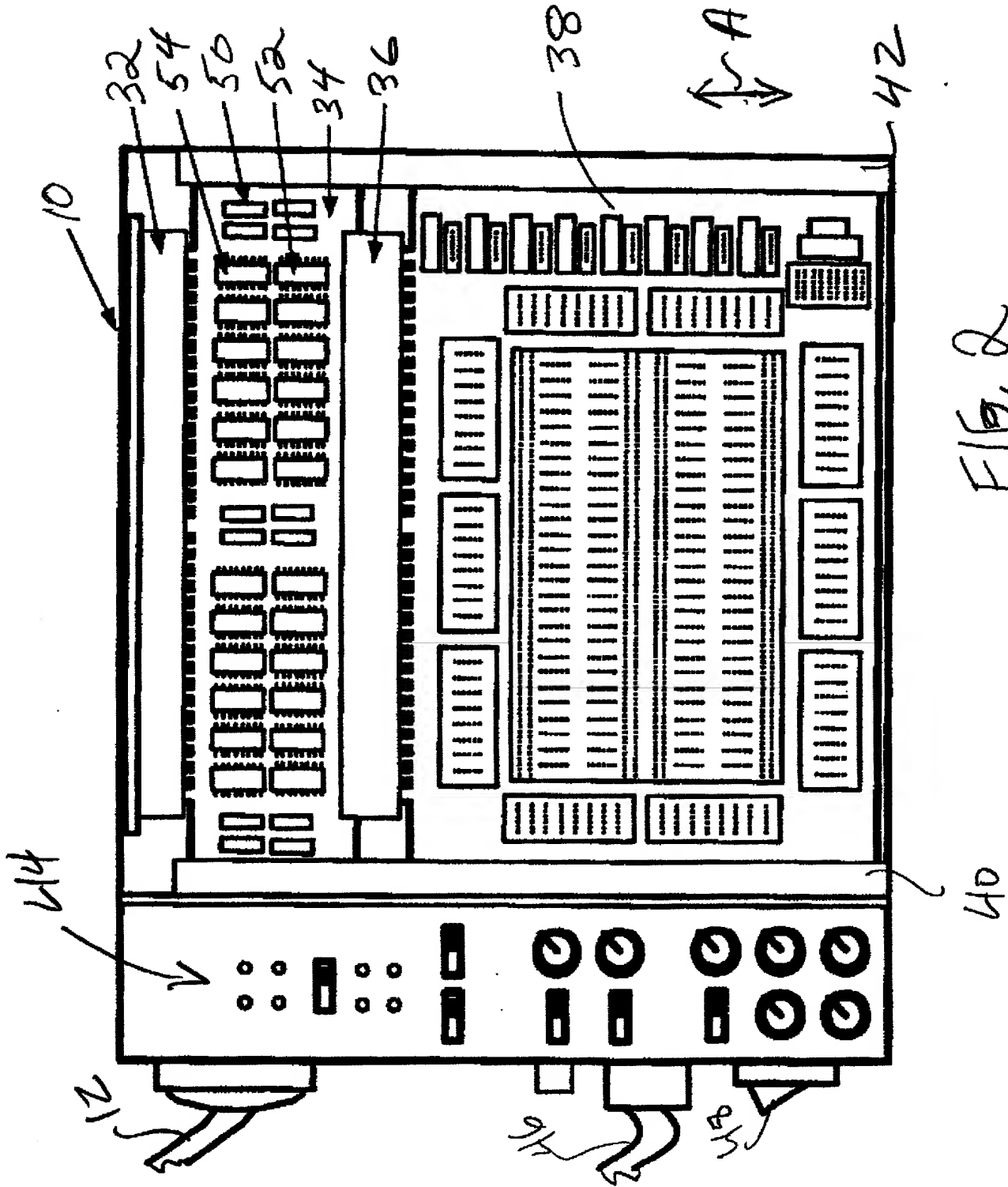
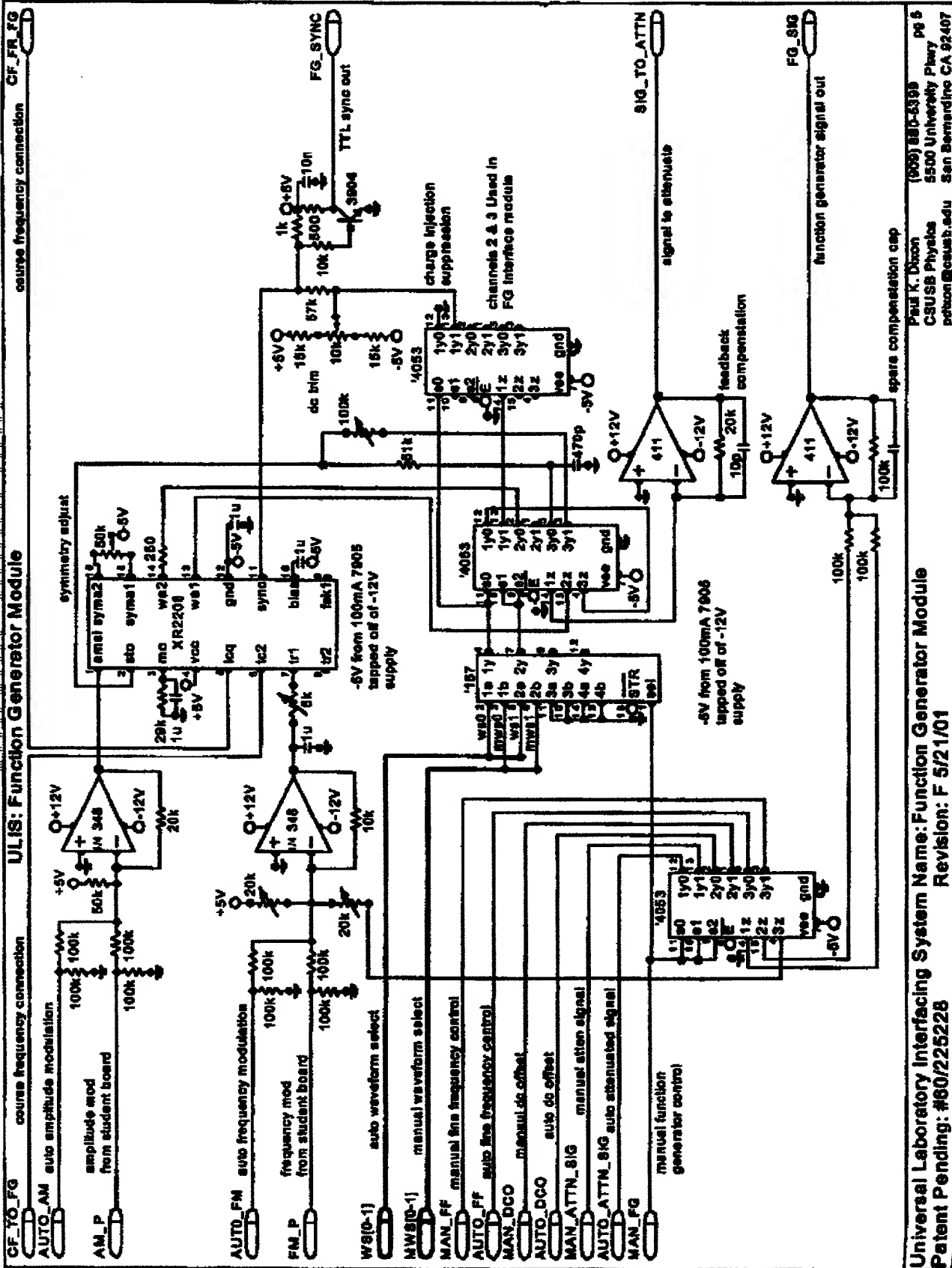


FIG. 2



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pg 6

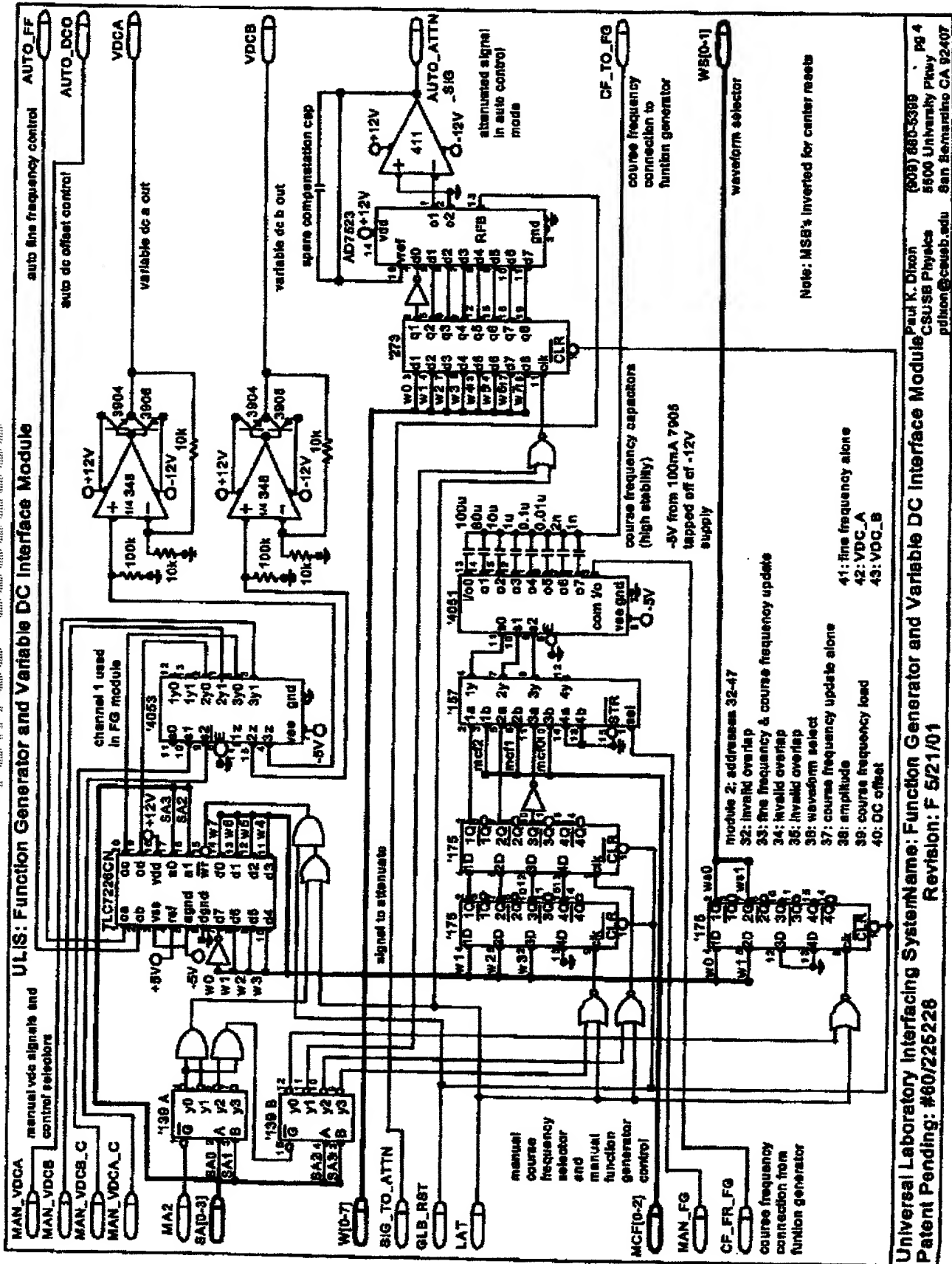
Fig. 4



F16.5

ULIS: Function Generator and Variable DC Interface Module

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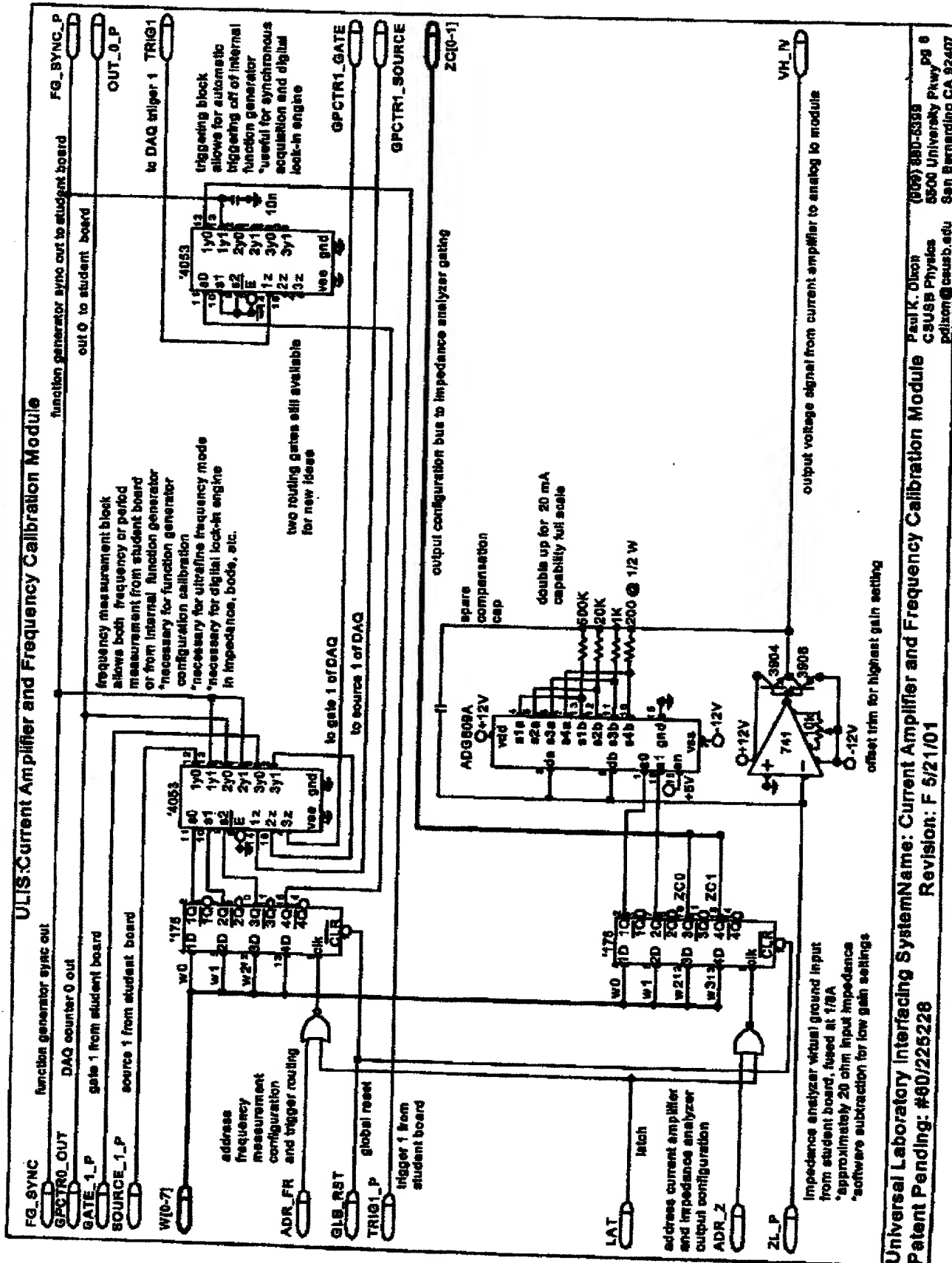
F16.6

Universal Laboratory Interfacing SystemName: Function Generator and Variable DC Interface Module Paul K. Dixon (805) 880-5399 pg 4  
Patent Pending: #80/225228 CSUSB Physics 5500 University Pkwy  
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Figure 1 consists of 12 histograms, labeled  $k=1$  through  $k=12$ , arranged horizontally. Each histogram shows the frequency of the number of non-zero elements in the vector  $x_k$ . The x-axis for all histograms is 'Number of non-zero elements' with ticks at 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10. The y-axis is 'Frequency' with ticks at 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10. The distributions are roughly bell-shaped and centered around 5-6 non-zero elements.



Universal Laboratory Interfacing System      Name: Analog Input/Output Module  
Patent Pending: #80/225228      Revision: F 5/21/01





Variable	Mean	SD	Min	Max
Age	34.5	10.2	21	55
Gender	0.5	0.5	0	1
Marital status	0.6	0.5	0	1
Education	12.5	1.5	9	16
Income	15.2	5.8	5	35
Health status	0.8	0.4	0	1
Smoking status	0.3	0.5	0	1
Alcohol consumption	0.2	0.4	0	1
Exercise frequency	0.5	0.5	0	1
Stress level	4.2	1.8	1	7
Sleep quality	0.7	0.5	0	1
Work satisfaction	0.6	0.5	0	1
Life satisfaction	0.8	0.4	0	1
Depression score	1.5	1.2	0	4
Anxiety score	1.2	1.0	0	4
Overall well-being	0.7	0.5	0	1

power and ground connections

direct to earth ground    GND    GND\_SS    student board ground plane

GND\_DAQ\_AI    GND\_DAQ\_AI\_SS    tie points across

+5V\_P    1.5A fast    +5V\_SS

+12V\_P    1.5A fast    +12V\_SS

-12V\_P    1.5A fast    -12V\_SS

power connections on main board

power connections on student board side of protection board

analog out large signal connections

main board    +12V\_M    1/8A fast    ANALOG\_LS\_P    ANALOG\_LS\_SS    -12V\_M

signals: A00 AO1 VDCA VDCB ZH ZM ZL

board presence connections

main +5V and ground    PB\_PRE    100k    PB\_PRE\_P    SS\_PRE    100k    SS\_PRE\_P    student board

high on connection    Internal

these internal connections make no contact to student board power or ground

identifiers

internal    SS\_PIO-7    100k    +5V\_SS    student board

Board identifier bits    100k    GND\_SS    student board

100k bussed resistors    100k

power and ground connections

direct to earth ground    GND    GND\_SS    student board ground plane

GND\_DAQ\_AI    GND\_DAQ\_AI\_SS    tie points across

+5V\_P    1.5A fast    +5V\_SS

+12V\_P    1.5A fast    +12V\_SS

-12V\_P    1.5A fast    -12V\_SS

power connections on main board

power connections on student board side of protection board

analog out large signal connections

main board    +12V\_M    1/8A fast    ANALOG\_LS\_P    ANALOG\_LS\_SS    -12V\_M

signals: A00 AO1 VDCA VDCB ZH ZM ZL

board presence connections

main +5V and ground    PB\_PRE    100k    PB\_PRE\_P    SS\_PRE    100k    SS\_PRE\_P    student board

high on connection    Internal

these internal connections make no contact to student board power or ground

identifiers

internal    SS\_PIO-7    100k    +5V\_SS    student board

Board identifier bits    100k    GND\_SS    student board

100k bussed resistors    100k

analog small signal connections

main board    +12V\_M    100    ANALOG\_SS\_P    ANALOG\_SS\_SS    -12V\_M

signals: AIO-13 AISENSE PG\_SIO AM FM

some direct to DAQ, others thru main circuit

volumeter connections

+12V\_M    800k    VOLT\_METER\_P    VOLT\_METER\_SS    -12V\_M

all diodes on main board

signals: VH VL

digital connections

+5V\_M    100    DIGITAL\_P    DIGITAL\_SS    GND\_M

signals: SYNC\_OUT WSP-7 ASIO-4 RS(S-7) PFIO-M CRT0\_OUT CRT1\_OUT SD\_CLK EXT\_STR FREQ\_OUT

some direct to DAQ, others thru main circuit

General purpose analog/digital prototyping board has identifier: 00000001

hard-wired connections defining model number of student board: 00000000 invalid 11111111 invalid

all resistors in 16 pin DIP isolated package 300mW ceramic substrate (CTS 781-3-3)

300 mA minimum current rating on all diodes

all diodes on main board

FIG. 9

Universal Laboratory Interfacing System      Name: Protection Module  
Patent Pending: #80/225228      Revision: F 5/21/01

Parameter	Unit	Value	Standard Error	t-Statistic	p-Value
Intercept		1.0000	0.0000	1.0000	0.0000
Age	Years	0.0000	0.0000	0.0000	0.0000
Gender		0.0000	0.0000	0.0000	0.0000
Marital Status		0.0000	0.0000	0.0000	0.0000
Education	Years	0.0000	0.0000	0.0000	0.0000
Income	\$/Year	0.0000	0.0000	0.0000	0.0000
Health		0.0000	0.0000	0.0000	0.0000
Smoking		0.0000	0.0000	0.0000	0.0000
Alcohol		0.0000	0.0000	0.0000	0.0000
Exercise		0.0000	0.0000	0.0000	0.0000
Stress		0.0000	0.0000	0.0000	0.0000
Family Size		0.0000	0.0000	0.0000	0.0000
Work Hours	Hours/Week	0.0000	0.0000	0.0000	0.0000
Job Satisfaction		0.0000	0.0000	0.0000	0.0000
Life Satisfaction		0.0000	0.0000	0.0000	0.0000
Residual Sum of Squares		0.0000	0.0000	0.0000	0.0000
Adjusted R-Square		0.0000	0.0000	0.0000	0.0000
F-Statistic		0.0000	0.0000	0.0000	0.0000
Prob(F-Statistic)		0.0000	0.0000	0.0000	0.0000

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**Name: Addressing, Digital I/O and Status Module**  
**Revision: F 5/21/01**

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**Universal Laboratory Interface  
Patent Pending: #60/225228**

Fig. 10

